MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

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MICROMACHINED STIMULATING MICROELECTRODE ARRAYS

Summary

This contract seeks to develop a family of thin-film stimulating arrays for use in neural prostheses. STIM-2B/-3B are two- and three-dimensional arrays of stimulating sites on 400μm centers. The probes have four channels and 64-sites. Any selected site can be used for either recording or stimulation. Current generation is off-chip. The high-end probes STIM-2/-3 are similar except they use on-chip current generation via 8-bit digital to analog converters.

Recent activities in the development of these active stimulating probes have focused on the external probe interface system and hardware. The graphical user interface (GUI) and probe drivers were updated to enable addressing of the 3D STIM-3B arrays in addition to the STIM-2B probes. The GUI prompts the user for the number of probes in the 3D array and configures the system accordingly. The input X- and Y-address data used to select the probe and the site on that probe are padded with extra bits to ensure they are of the same length and that the addresses will align properly in the input shift registers for reliable selection. Additional improvements are also being made to the software to make the system easier to use, in preparation for providing the system to outside users.

As part of the external probe stimulating system, a hardware interface has been built to facilitate current generation and recording on the headstage, avoiding the high distributed capacitance of the cables between the external system and the preparation. The circuitry was designed and built on a printed circuit board (PCB). Current sources, a recording buffer, and a probe power supply current monitor were all included on the PCB for added flexibility and monitoring capability. The circuitry performs voltage-to-current conversion to generate the stimulus currents for STIM-2B/-3B, ensures charge-balancing, and provides a high drive impedance along with bias stabilization in recording mode. The output drive impedance (input recording impedance) as seen from the site is set by a fixed 100MΩ bias resistor. During the coming quarter, we expect to use the hardware interface to complete series of long term *in-vitro* pulse tests and to use it in *in-vivo* stimulation and recording experiments.

We are also continuing the final design optimization of STIM-2 and have explored a new self-balancing design for the digital-to-analog current sources needed for that probe. Dedicated data lines to permit recording during stimulation have been added along with a DAC to permit the use of up to 8 levels of anodic and cathodic bias on unused sites. The STIM-2 design should be completed during the coming term. STIM-3 will then be designed so that both probes can be fabricated before the end of the year. We are also beginning the design of a telemetry interface that will permit these probes to be operated over an rf power/data link, eliminating the need for a hardwired interface and percutaneous plug.

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1. Introduction

The goal of this contract is the development of active multi-channel arrays of stimulating electrodes suitable for studies of neural information processing at the cellular level and for a variety of closed-loop neural prostheses. The probes should be able to enter neural tissue with minimal disturbance to the neural networks there and deliver highly-controlled (spatially and temporally) charge waveforms to the tissue on a chronic basis. The probes consist of several thin-film conductors supported on a micromachined silicon substrate and insulated from it and from the surrounding electrolyte by silicon dioxide and silicon nitride dielectric films. The stimulating sites are activated iridium, defined photolithographically using a lift-off process. Passive probes having a variety of site sizes and shank configurations have been fabricated successfully in past contracts and have been distributed to a number of research organizations nationally for evaluation in many different research preparations. For chronic use, the biggest problem associated with these passive stimulating probes concerns their leads, which must interface the probe to the outside world. Even using silicon-substrate ribbon cables, the number of allowable interconnects is necessarily limited, and yet a great many stimulating sites are ultimately desirable in order to achieve high spatial localization of the stimulus currents.

The integration of signal processing electronics on the rear of the probe substrate (creating an "active" probe) allows the use of serial digital input data which can be de-multiplexed on the probe to provide access to a large number of stimulating sites from a very few leads. Our goal in this area is to develop a family of active probes capable of chronic implantation in tissue. For such probes, the digital input data must be translated on the probe into per-channel current amplitudes that are then applied to the tissue through the sites. Such probes generally require five external leads, virtually independent of the number of sites used. As discussed in previous reports, we have designed a series of active probes containing CMOS signal processing electronics. Two of these probes have been completed and are designated as STIM-1A and STIM-1B. A third probe, STIM-2, is now beginning a final iteration and is a second-generation version of our original high-end first-generation design, STIM-1. All three probes provide 8-bit resolution in digitally setting the per- channel current amplitudes. STIM-1A and -1B offer a biphasic range using ±5V supplies from 0μA to ±254μA with a resolution of 2μA, while STIM-2 has a range from 0 to ±127μA with a resolution of 1μA. STIM-2 offers the ability to select 8 of 64 electrode sites and to drive these sites independently and in parallel, while STIM-1A allows only 2 of 16 sites to be active at a time (bipolar operation). STIM-IB is a monopolar probe, which allows the user to guide an externally-provided current to any one of 16 sites as selected by the digital input address. The high-end STIM-2 contains provisions for numerous safety checks and for features such as remote impedance testing in addition to its normal operating modes. It also offers the option of being able to record from any one of the selected sites in addition to

stimulation. It will be the backbone of a multi-probe three-dimensional (3D) 1024-site array (STIM-3) now in development. A new probe, STIM-2B, has recently been added to this set. It offers 64-site capability with off-chip generation of the stimulus currents for four separate channels. These channels are organized in four groups so that each current can be directed to any of the 16 sites in its group. Each selected channel can be programmed for either stimulation or recording. On-chip recording amplifiers offer a gain of 50; alternatively, the neural activity can be recorded using off-chip amplifiers interfaced through the normal stimulating channels. This probe is available in both 2D and 3D versions (as STIM-2B/3B) and is now being used in-vivo.

During the past quarter, we have continued to fabricate passive probe structures for a variety of users. We have also improved the graphical user interface associated with the external control system for use with these probes, allowing them to now handle 3D arrays. A headstage-mounted hardware interface has also been realized to provide the necessary current generation and buffering of recorded signals from the probe. Work is underway on the redesign of STIM-2 and the design of a telemetry interface for use with the probes. The results in each of these areas are described more fully in the sections below.

2. Active Stimulating Probe Development

Recent activities in the development of active stimulating probes have focused on the external probe interface system and hardware. The graphical user interface and probe drivers were updated to enable addressing of the 3D STIM-3B arrays in addition to the STIM-2B probes. The circuitry for a cable terminator/probe connector was designed and built on a printed circuit board (PCB). Current sources, a recording buffer, and a probe power supply current monitor were all included on the PCB for added flexibility and monitoring capability.

STIM-2B

STIM-2B is a four-channel, 16-shank, 64-site probe which routes four externally generated stimulus signals to 1-of-16 sites per channel. The fabrication of the CMOS circuitry has been completed and the functionality of the circuitry has been verified by testing the different modes of the probe: POR, site selection, amplifier selection, and so forth. Testing of the analog amplifier has demonstrated that it works quite well *in-vitro*, though *in-vivo* operation has been problematic due to large DC drifts at the iridium sites.

The STIM-2B probe is expected to provide a badly-needed tool for performing some very important experiments, allowing acute and chronic stimulation access to a relatively large volume of neural tissue without mechanically repositioning of the probe. This capability is realized by utilizing a 20b shift register to load four 4b site addresses, which are decoded by a 1-of-16 nand-type decoder to connect the desired site to an analog input/output pad through a large CMOS passgate transistor. This allows the ‘steering’ of externally-generated currents to the addressed site. A recording function is

included and is addressed by a fifth bit included with the 4b site address. This fifth bit selects between stimulation mode and recording mode by selecting either a direct path to the I/O pad from the site or a path through an amplifier to allow recording from the same site. Each I/O channel has its own dedicated amplifier so that the functionality of each channel is independent of the others except for the up-front data input circuitry.

STIM-3B

The logical extension of STIM-2B is to make it into a three-dimensional (3D) array. This was done to realize STIM-3B. STIM-3B is set up in a platform configuration with an integrated ribbon cable for connection to a percutaneous plug, allowing use of the device in chronic experiments. The differences between STIM-2B and –3B are some structural modifications to allow interconnection to a 3D-platform assembly and a few additional circuit blocks to facilitate the addressing of multiple probes in a 3D array.

As in the STIM-2B design, the STIM-3B probe is a four-channel, 16-shank, 64-site probe which routes four externally-generated stimulus signals to 1-of-16 sites per channel. In order to allow addressing of multiple probes in a 3D array, STIM-3B has an extra 4b serial input shift-register which, when the bits are set, connects the corresponding I/O channel of the probe onto a common I/O bus on the platform. All of the extra registers of the probes in a STIM-3B array are connected in series via platform leads to form an extended or virtual register. The virtual register enables all of the probes in the 3D array to be addressed with only two address lines, a channel enable address line (X-ADDR), and a site address line (Y-ADDR). This architecture does have a limitation in that it does not allow independent use of the same site address on two separate probes in the array. The slightly reduced flexibility was considered a reasonable sacrifice to achieve a reduction in circuit complexity and lead count.

The addressing of STIM-3B is somewhat different than STIM-2B; therefore, we were not previously able to operate the STIM-3B probes with the external interface system that we have developed. It is necessary to simultaneously load the Y-ADDR data and the X-ADDR data, which may be of different lengths depending on the number of probes being addressed. The Y-ADDR data word is always 20b long. The X-ADDR data word can vary from 4b for a single-probe array up to 64b for a 16-probe array. The important criteria in entering the data is that both data words complete loading at the same time no matter which data word is longer so that the data words are properly aligned. It is thus necessary to pad the shorter data word with dummy data at the beginning so that the desired data is entered at the proper time. It is also important that the termination of the clock pulses is synchronized with the end of both data words. If the clock should continue pulsing after the data words are complete, something will continue to be loaded, whether it is correct or not. Thus it is important to ensure that the data words are properly synchronized with each other and with the clock. Note, that one complicating factor is that the actual data words as stored in the RemStim sequencer are actually five bits; therefore, the number of clock cycles is always a multiple of five. In spite, of the complexities, the completed system works quite well.

A designator for the number of probes in a 3D array was added to the Probe Configuration pop-up window, as shown in Fig. 1. The allowable array sizes range from a single-probe array to a 16-probe array. This is probably the largest array that will be used in the near future, but if necessary, this can be easily changed if a larger array size is indeed desired. As it turns out, it is not necessary to distinguish between the STIM-2B and STIM-3B probes since the same protocol used for a single STIM-3B probe array is compatible with the STIM-2B array. The X-ADDR data line is simply not connected and is therefore ignored. The proper addressing protocol is generated when the OK button of the Probe Configuration window is clicked. It is then necessary to 'Reset' the RemStim board so that the sequencer protocol is downloaded to the RemStim board. The user is reminded to do this by a separate window that pops up. The GUI and the RemStim board now both know how to properly address the designated array size.

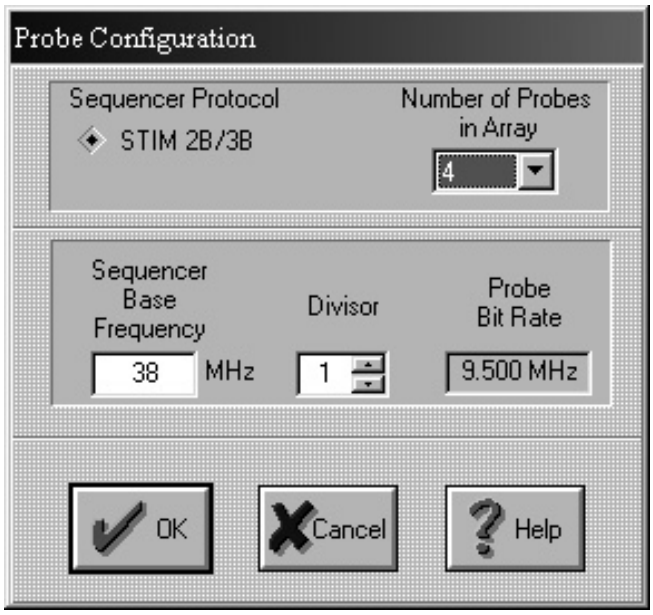

Fig. 1: The pop-up Probe Configuration window which, among other things, allows the user to define the number of arrays present in a 3D array. Selecting one probe will operate either a STIM-2B probe or a single STIM-3B probe array.

The main GUI window, Fig. 2, has also been updated to accommodate the addressing of different probes in a 3D array. In each channel, a 'Probe #' can be specified such that the channel will be active on the probe specified. The 'Probe #' will not allow the user to select a probe number larger than the array size. Whenever the 'Number of Probes in the Array' is changed in the Probe Configuration window, the menus of the main window are updated to reflect the size of the designated array (in this case 4); therefore, the user cannot choose an illegal (nonexistent) probe unless the array size was improperly specified.

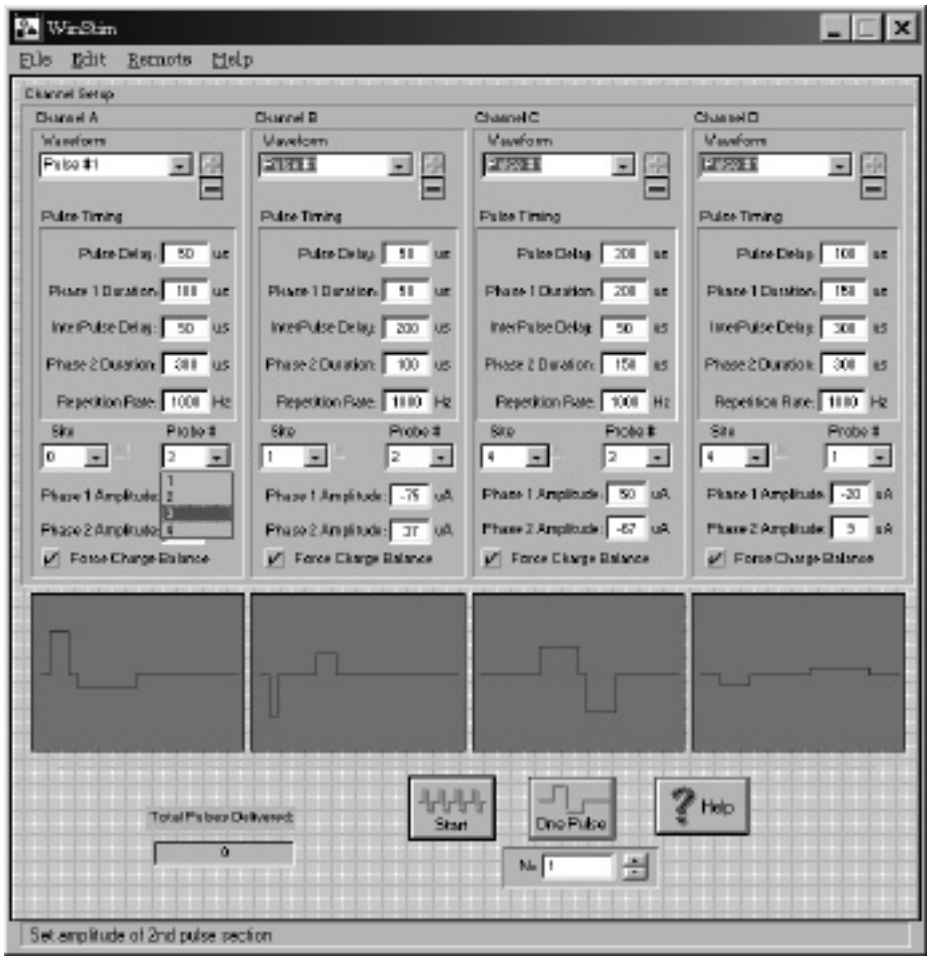

Fig. 2: The main user interface window now allows the user to define which probe in a 3D array each channel is to be routed to. The number of probes is defined in the probe configuration window and only probes within the defined size can be selected as can be seen in the drop-down menu of the Probe # of Channel A.

Figures 3 and 4 demonstrate how the data signals change for different size arrays. The overshoot and ringing noted in these traces are due to improper impedance matching at the oscilloscope inputs. Figure 3 shows how a single-probe array is addressed. The X-ADDR data is padded until it ends with the end of the clock sequence. Figure 4 demonstrates, with a six-probe array address, what happens when the X-ADDR data word is larger than the Y-ADDR, requiring that it be padded at the beginning.

The external user interface system is continuously being updated as new features are needed. There are several more changes that are currently pending, such as making the ‘tick interval’ more easily user definable. The ‘tick interval’ is the minimum resolution with which the current pulses can be defined. It also makes sense to force the duration times to coincide with this ‘tick interval’ when the software does charge

balancing, but this is not currently the case and the user must be careful to correct this. There continue to be small things such as this that we are continuing to modify to make the system easier to use. A major change that is still pending is the support of the full STIM-2 addressing protocol. The support for this probe will require significant changes in the operating scheme since here the data being sent to the probe updates the current levels directly rather than having the current updates done on the external RemStim board itself, as in STIM-2B/3B.

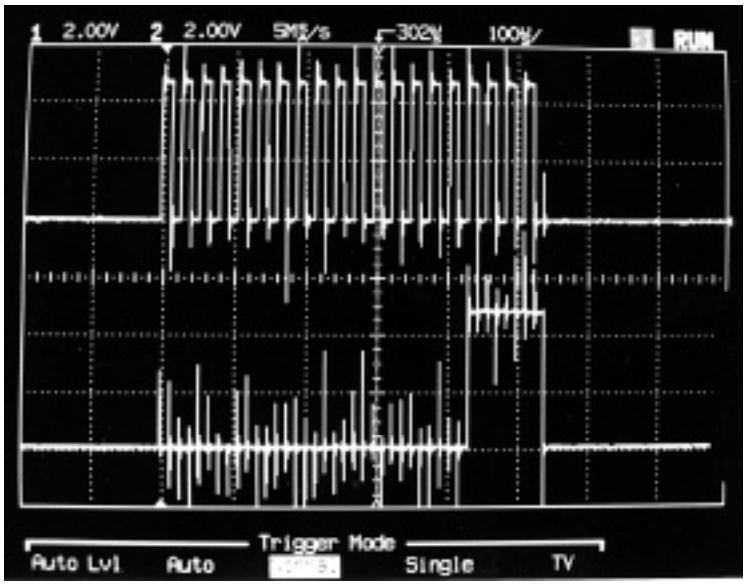

Fig. 3: The top scope trace is the clock and the bottom is the X-ADDR data for an array of one probe. Note, that even with a single-probe array, at least 20 clock cycles are required in order to enter the site address data.

Cable Termination/Probe Connector Design and Development

As discussed in a previous quarterly progress report, we decided to include a voltage-to-current converter circuit (current source) on the probe connector as well as circuits for monitoring the probe power supply currents and direct recording from the STIM-2B/3B sites. While the circuits are not complex, some of the tasks, particularly the simultaneous recording capability, place stringent performance requirements on them. These circuits have been designed and implemented in a small surface-mount printed circuit board (PCB).

A block diagram, as presented in a previous quarterly progress report, is shown below in Fig. 5. The RemStim board handles all of the digital and analog signal generation needed to operate the STIM-2B/3B probes. As discussed above, the RemStim user interface has been upgraded to be able to seamlessly handle either the 2D STIM-2B or the 3D STIM-3B probe array data protocols by simple specifying the number of probes

present in the array being used. First of all, the connector board provides the necessary 75Ω termination of the high-speed digital clock and address data lines. The termination is necessary because of the 75Ω impedance of the Sun Video cable's mini-coax lines. The next important feature is the current source for generating the current stimulus waveforms. The current source, a voltage-to-current converter, is driven by a voltage signal which is generated by the RemStim board's D/A converters. Although the RemStim board was designed to accept a current-source-output daughter board, because of the relatively large shunt capacitance of the Sun Video cable, we decided to move the current-source circuitry out closer to the probe. This improves the performance of the current sourcing circuitry since less of the current is 'lost' to charging the shunt capacitance of the long cable.

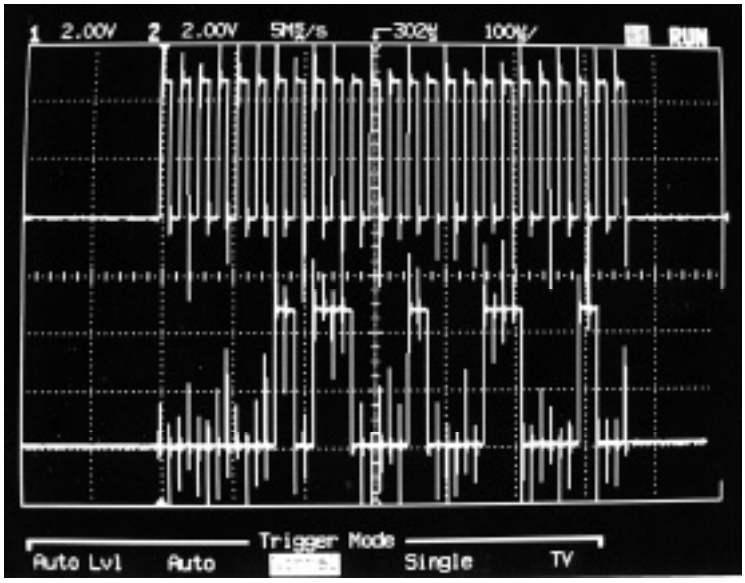

Fig. 4: The top scope trace is the clock and the bottom trace is the site address data for an array of six probes. Note that now 25 clock cycles are used (24 are needed for the X-DATA, but 5b words are used), but only 20 are needed for the Y-ADDR; therefore, the first five clock cycles are padded to ensure the end of the clock and address data are synchronized.

A unity gain buffer is also included on the connector to buffer any recorded signals, including neural spike activity and back-voltages due to stimulation. This was a challenging proposition since it is necessary to record the signals from the same node as the output of the current source. The key is to maintain a very high impedance at this node so that small neural signals are not attenuated while possibly very high (full scale, supply rail) voltages generated at high current stimulation levels can be handled, all the while operating from the ±5V rails common to the probe.

Finally, three power-supply current-monitoring circuits for ±5V and ground of the probe were designed. These circuits are included to ensure that the probe is not developing any current leakage paths during *in-vitro* testing or *in-vivo* use. The circuits only monitor the current that is actually being delivered to the probe, not what is being used by the connector board circuits.

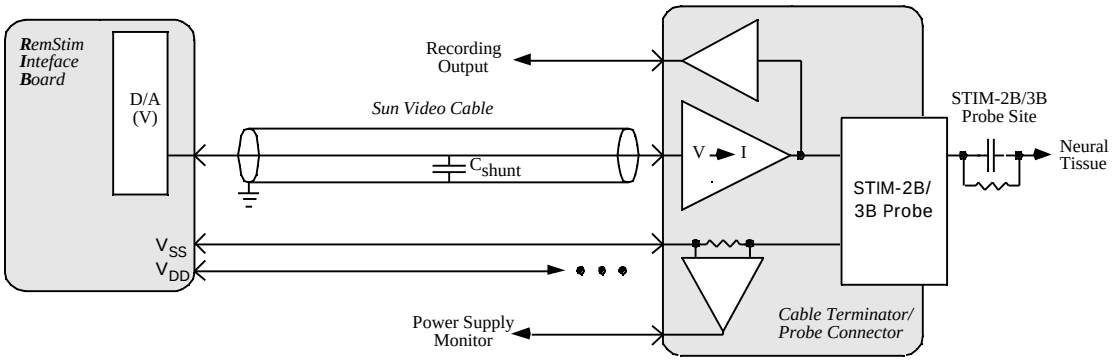

Fig. 5: The block diagram of the external system for operating the probes, including the generation of current stimuli, the monitoring of probe power consumption and the recording of neural signals and/or site voltage characteristics during stimulation.

The circuit diagram of the connector current source is shown in Fig. 6. This circuit was originally developed for use as a current source in iontophoresis. The present configuration is altered slightly from the original in order to make it a non-inverting voltage-to-current converter and to provide self-compensation of any input offset voltage in the opamp. The output resistance of the current source is given by:

$$R_{out} = \frac{R_f\left(1 + A_v\left(\frac{R_3}{R_3 + R_4}\right)\right)}{1 + A_v\left(\frac{R_3}{R_3 + R_4} - \frac{R_1}{R_1 + R_2}\right)}$$

and if $R_1 = R_3$ and $R_2 = R_4$, then the equation reduces to:

$$R_{out} = R_f\left(1 + A_v\left(\frac{R_3}{R_3 + R_4}\right)\right)$$

From this equation, we see that R_{out} is primarily determined by matching the resistors and then by maximizing the gain of the opamp, A_v. For the implementation of this circuit, 0.1% resistors were used for R_2 and R_4 and 1% resistors were used for R_1 and R_3 (more precise resistors were not available in that size). By individually selecting R_1 and R_3, a very high output resistance could be achieved. In order to provide a DC path to ground, a 100MΩ biasing resistor shunts the output node to ground (Fig. 6). The goal is

to make this the dominant resistance. This can be achieved if the other impedances are at least an order of magnitude higher or >1GΩ. There is a small range for R_3 of ~100Ω in which the output resistance theoretically exceeds 1GΩ. With proper trimming of the circuit, the output resistance can go much higher. The unity-gain buffer in the positive feedback loop (as well as the recording output buffer) has a typical input bias current on the order of 80fA (maximum of 2pA); therefore, very little current is lost to either of these paths.

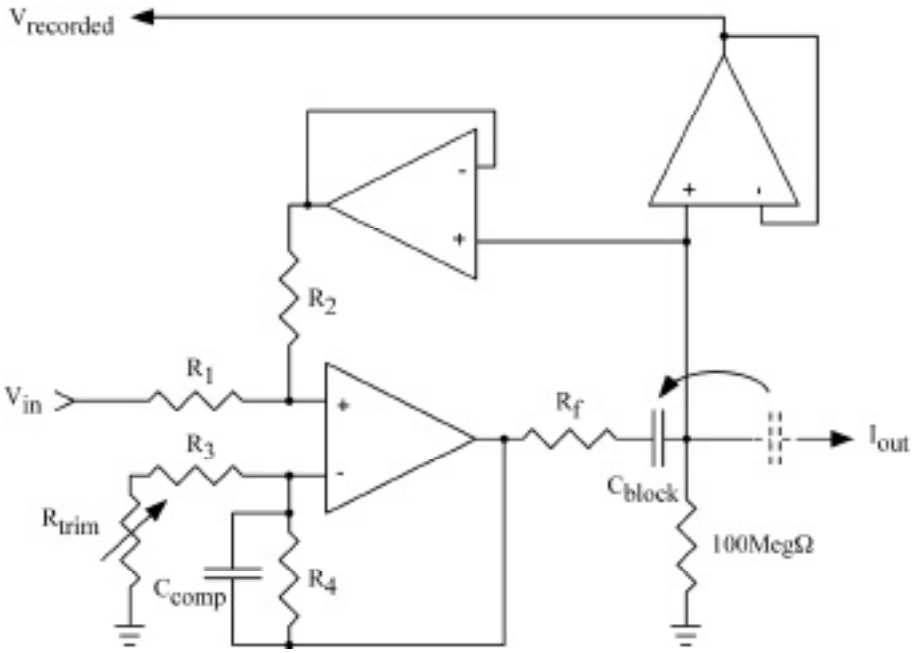

Fig. 6: The circuit diagram of the voltage-to-current converter including the unity gain recording output buffer.

The circuit was initially tested on a breadboard, and the output resistance was measured as shown in Fig 7. The I/V resistance measurements were only made over the range of a normal neural signal since it is primarily important for the output resistance to be maximized in this range. Figure 7 shows the results from a circuit that was trimmed very well, although the measurement was somewhat variable due to the low-level signals being measured in a noisy environment. Figure 8 shows how the actual signal looks when scaled.

The one important observation made was that there was a DC offset in the current, probably due to the input offset voltages of the opamp used. In most cases, current sources are coupled to the probe with large DC blocking capacitors in order to ensure charge-balanced pulses. The offset current driving into the high impedance output node quickly pushed to voltage at that node to the rail. One method of reducing this in the past has been to reduce the size of the 100MΩ bias resistor to allow the current a lower resistance path to ground. This has the effect of lowering the impedance seen by a

neural signal, attenuating it more. As an alternative with which to compensate the offset current here, the DC blocking capacitor was moved into the feedback loop as indicated by the arrow in Fig. 6. This feeds back any slight voltage that builds up due to DC current and compensates the input offset voltage of the opamp. With the DC blocking capacitor in the feedback loop and the100MΩ resistor in place, the output resistance measurement is as shown in Fig. 9. The current is centered around zero and the 100MΩ resistor dominates.

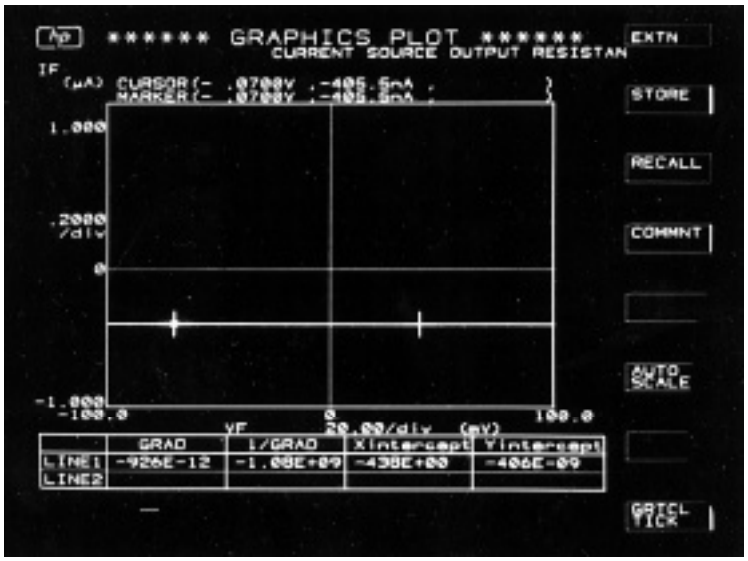

Fig. 7: The measurement of the output resistance, I_{out}/V_{out} (shown as 1/GRAD, the negative value is predicted by the equation for certain ranges) without the blocking capacitor in the feedback loop. Note, the offset current which can rapidly charge the output node with the blocking capacitor in the normal location.

The placement of the blocking capacitor in the feedback loop does have an effect on the output current, especially at high current levels over long time intervals as shown in Fig. 10. Because of the slight voltage build-up across the capacitor, the output current progresses towards zero, but this would be expected for this type of configuration. This does have the effect of ensuring that all pulses are charge balanced. It is not considered to be a problem since it is repeatable and is only really significant for large currents over long times. Figure 11 shows that the effects are much less for shorter time durations and lower current levels. If necessary, the effect can be reduced by simply increasing the size of the blocking capacitor.

The transient performance of the circuit is shown in Fig. 12 across a 46.4kΩ load. The difference between the response of Fig. 12 and that of Fig. 13, which has a 1kΩ load, indicates that there is some load sensitivity to the response time of the circuit. Rise and fall times on the order of 10µSec are considered to be quite sufficient for most current pulse stimulus patterns. The results of testing on the current source indicate that it should perform quite well for our purposes.

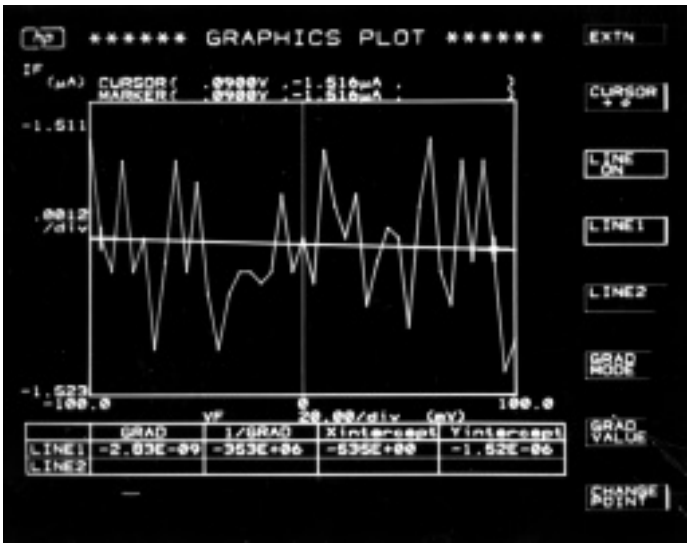

Fig. 8: A scaled measurement of the output resistance, I_{out}/V_{ou} (shown as 1/GRAD) which shows that the low current levels are down in the noise, but that a general slope can be established for an approximate output resistance measurement.

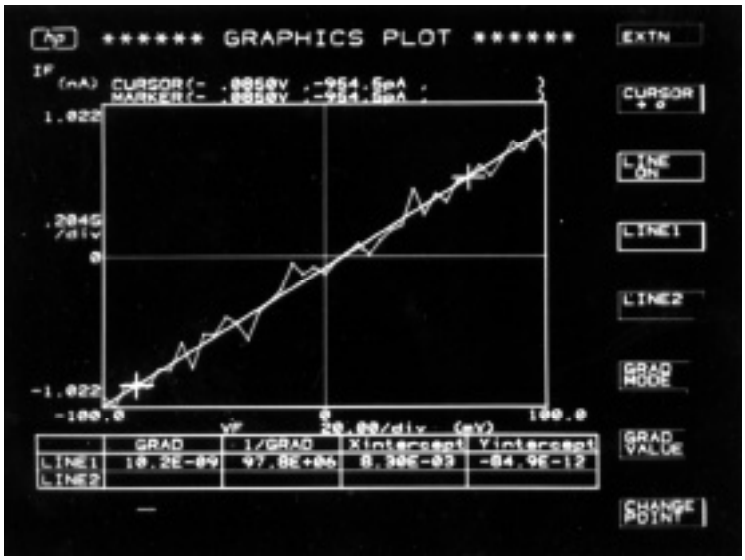

Fig. 9: A scaled measurement of the output resistance after trimming with the blocking capacitor and with the 100MΩ bias resistor in place. The 100MΩ bias resistor dominates the output resistance.

The positive power-supply current monitoring circuit is shown in Fig. 14. The circuit it quite simple, but works fairly well. The important thing is that the circuit only requires one opamp. Figure 15 shows the measured performance of the positive current supply monitor and compares it to the theoretical. There is a 200mV offset which is believed to be due to operation of the opamp near the positive rail in common mode. By

simply adding in the offset, the current can be measured very well. The circuits for the –5V current supply monitor and the ground current monitor are shown in Figs. 16 and 18, respectively. The measured characteristics are shown in Figs. 17 and 19, respectively, and indicate good behavior.

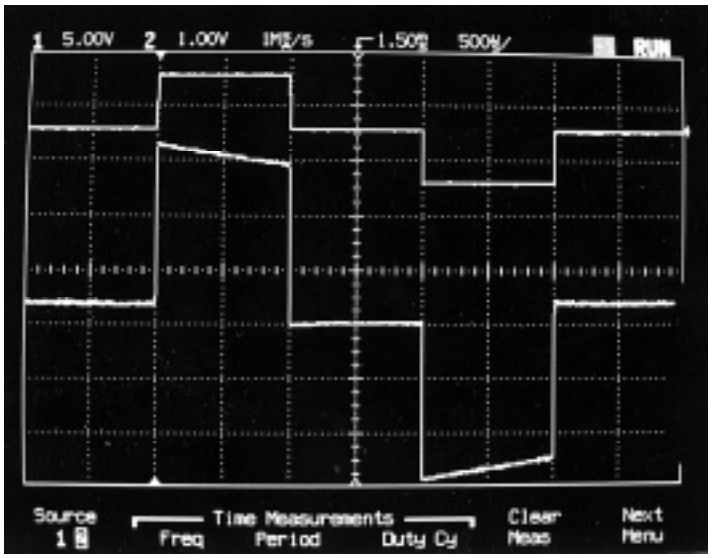

Fig. 10: The top trace is the driving voltage signal and the bottom trace is the current being driven across a resistor. This demonstrates the effect of the blocking capacitor in the feedback loop when driving high level currents for long periods of time.

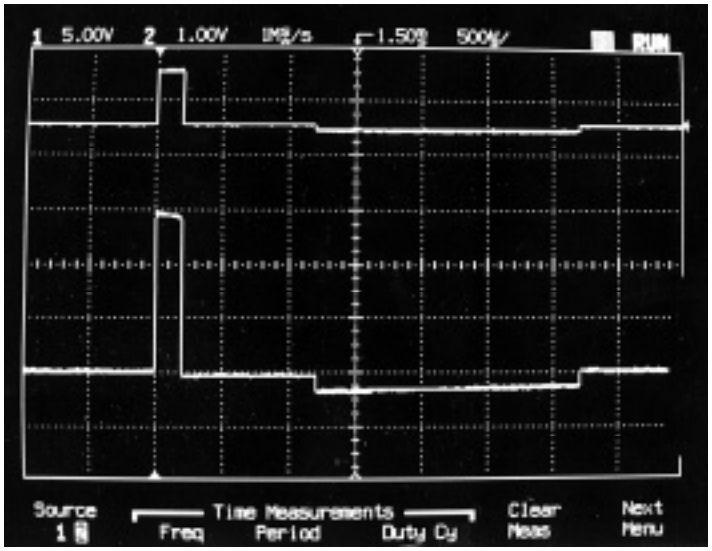

Fig. 11: The top trace is the driving voltage signal and the bottom trace is the current being driven across a resistor. This demonstrates the reduced effect of the blocking capacitor on short or low level current pulses, as was expected.

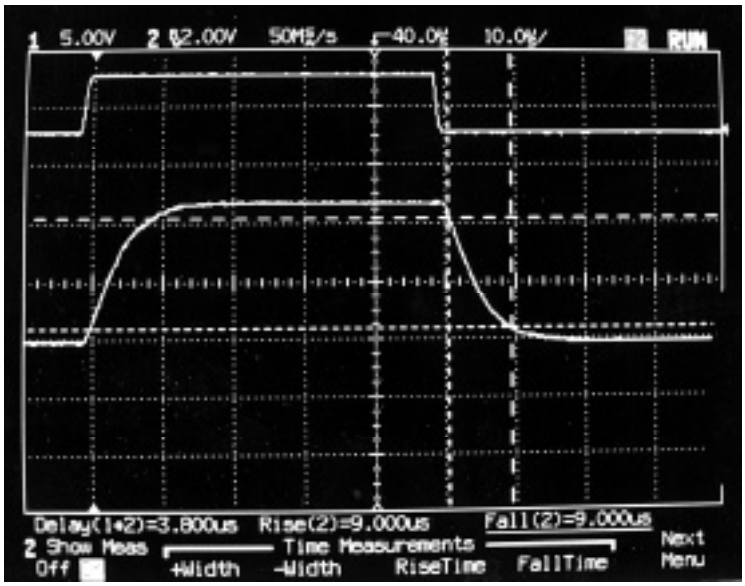

Fig. 12: The top trace is the driving voltage signal and the bottom trace is the current being driven across a 46.4kΩ load. The performance is fairly good with 9µSec rise and fall times and a 3.8µSec delay between driving signal and the output pulse.

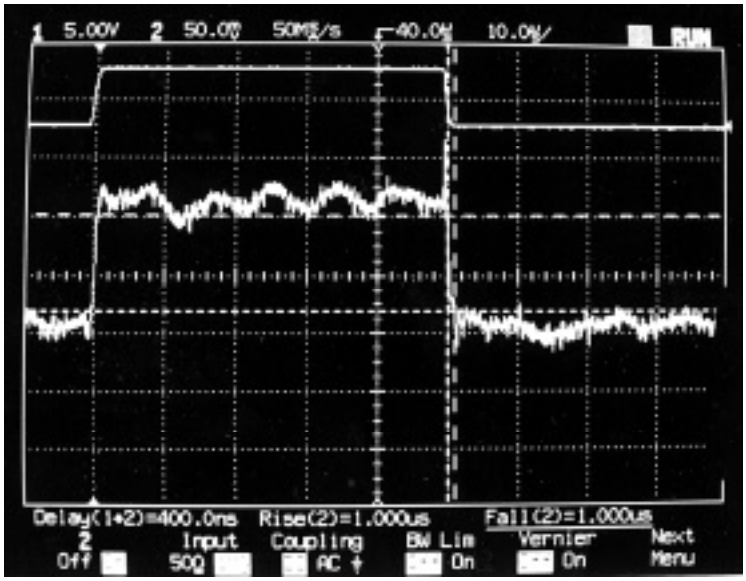

Fig. 13: The top trace is the driving voltage signal and the bottom trace is the current being driven across a 1kΩ load. The performance is very good with 1µSec rise and fall times and a 0.4µSec delay between driving signal and the output pulse.

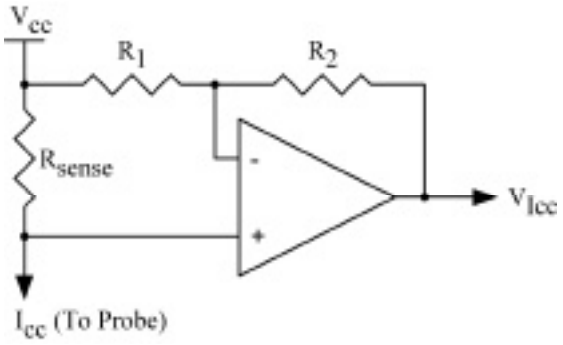

Fig. 14: The circuit used to monitor +5V current supplied to the probe.

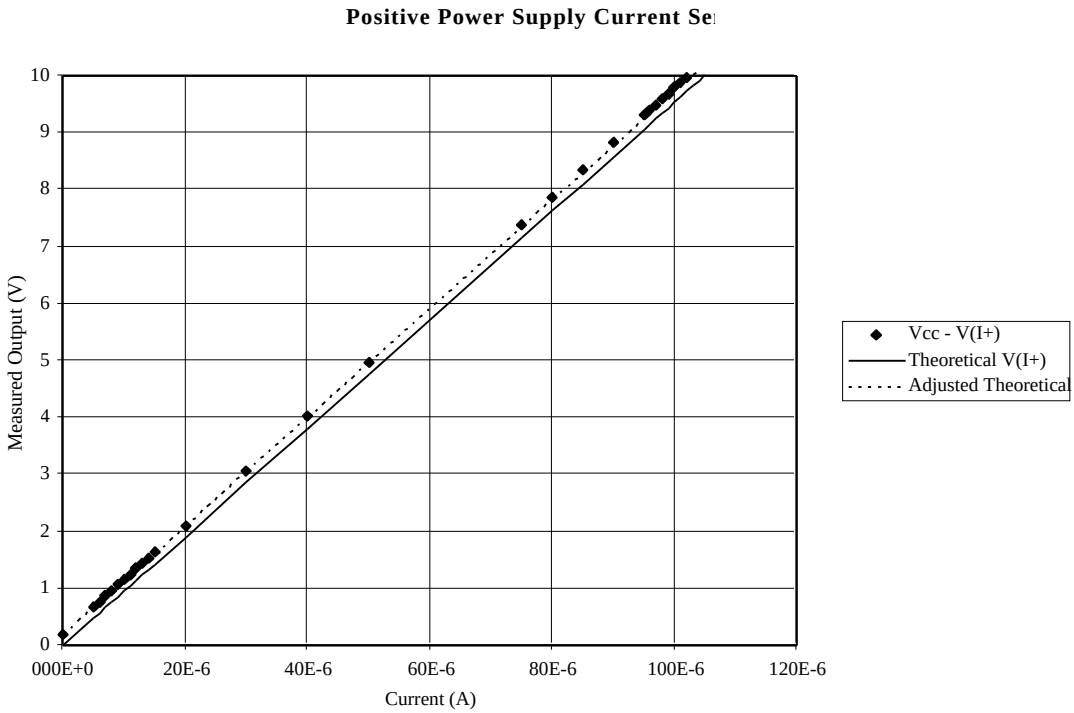

Fig. 15: The characterization of the +5V power supply monitoring circuit. The output is linear, but there is a slight offset believed to be due to operating the common mode input of the amplifier at the positive rail. The output can be easily matched by simple adding in the constant offset.

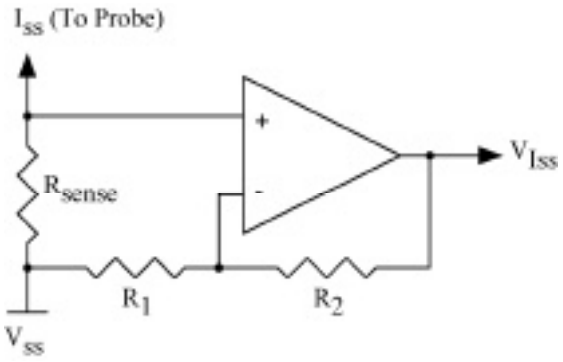

Fig. 16: The circuit used to monitor -5V current supplied to the probe.

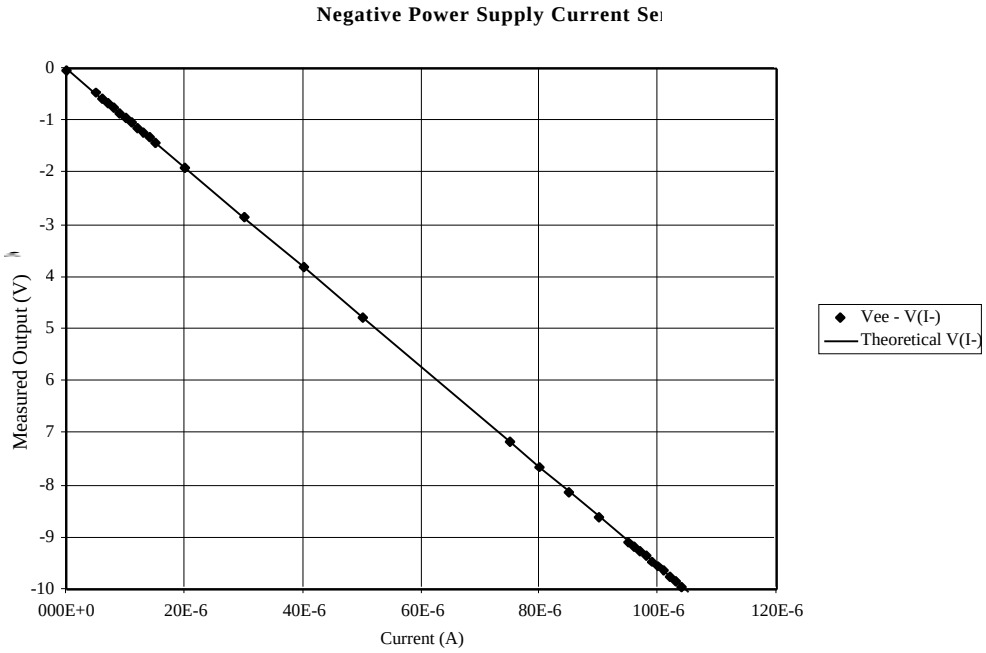

Fig. 17: The characterization of the –5V power supply monitoring circuit. The output matches very well with the theoretical calculations.

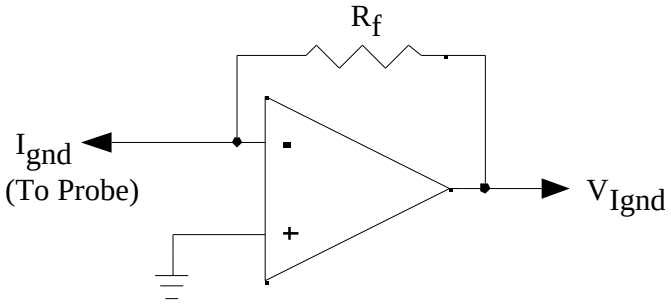

Fig. 18: The circuit used to monitor the ground current supplied to the probe, this uses a *virtual ground* for the probe ground.

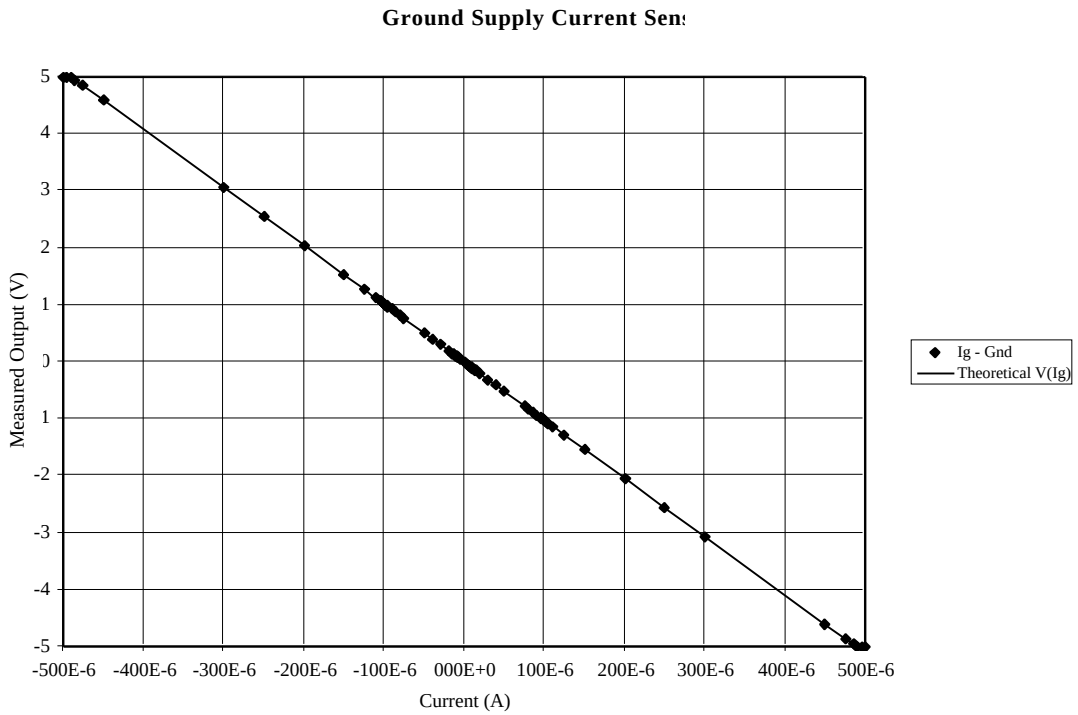

Fig. 19: The characterization of the ground supply monitoring circuit. The output matches very well with the theoretical calculations.

The circuits have been patterned on a PCB, and surface mount components were used to populate them as shown in Figs. 20 and 21. The overall size is somewhat larger than desired, but once the design has been shown to be effective in experiments, it can be fabricated commercially in a multilayer PCB with devices on both sides, thereby reducing the size by at least half. Figure 22 shows the back side of the PCB, which carries the power supply busses and the various connectors.

The completion of the cable terminator/probe connector has put into place the final piece needed to make this complete system very effective. The PCB will allow long term in-vitro pulse testing while monitoring site back-voltages and is expected to be very effective in *in-vivo* experiments for both stimulation and recording. Having both capabilities on the same board will allow us to locate the probes by recording and then also stimulate and observe the response.

During the past quarter, we have updated the user interface software to be able to address the STIM-3B arrays as well as the STIM-2B probes. We have also designed and built a very useful cable terminator/probe connector that gives extensive monitoring and recording capability in addition to the current sourcing. During the coming quarter, we expect to use the PCB to complete series of long term *in-vitro* pulse tests and to use it in *in-vivo* stimulation and recording experiments.

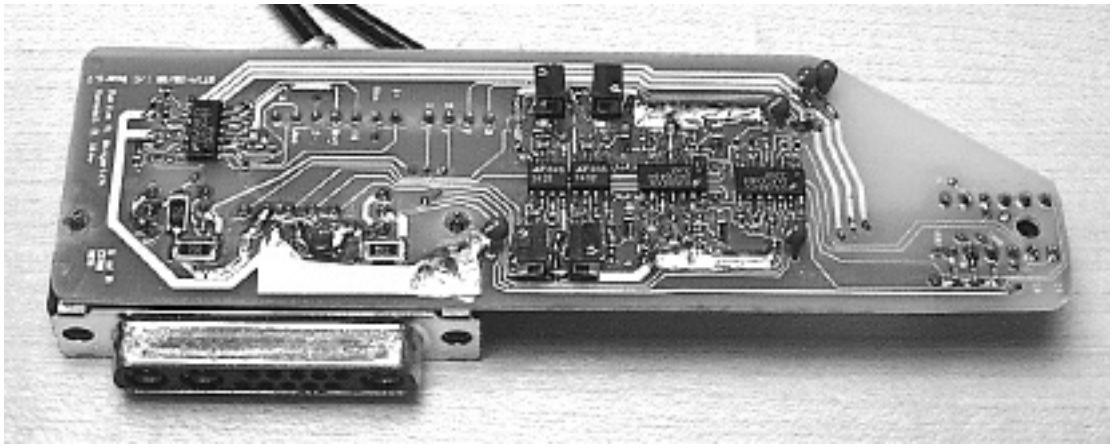

Fig. 20: A photograph of the completed cable terminator/probe connector PCB. Wherever possible, the devices are surface-mount devices in order to reduce the size. The recording buffer is located farthest to the right near the DIP for connecting the probe stalk (on the back side), then the current source IC's are located, and finally, the power supply monitoring circuits are positioned in the upper left hand corner.

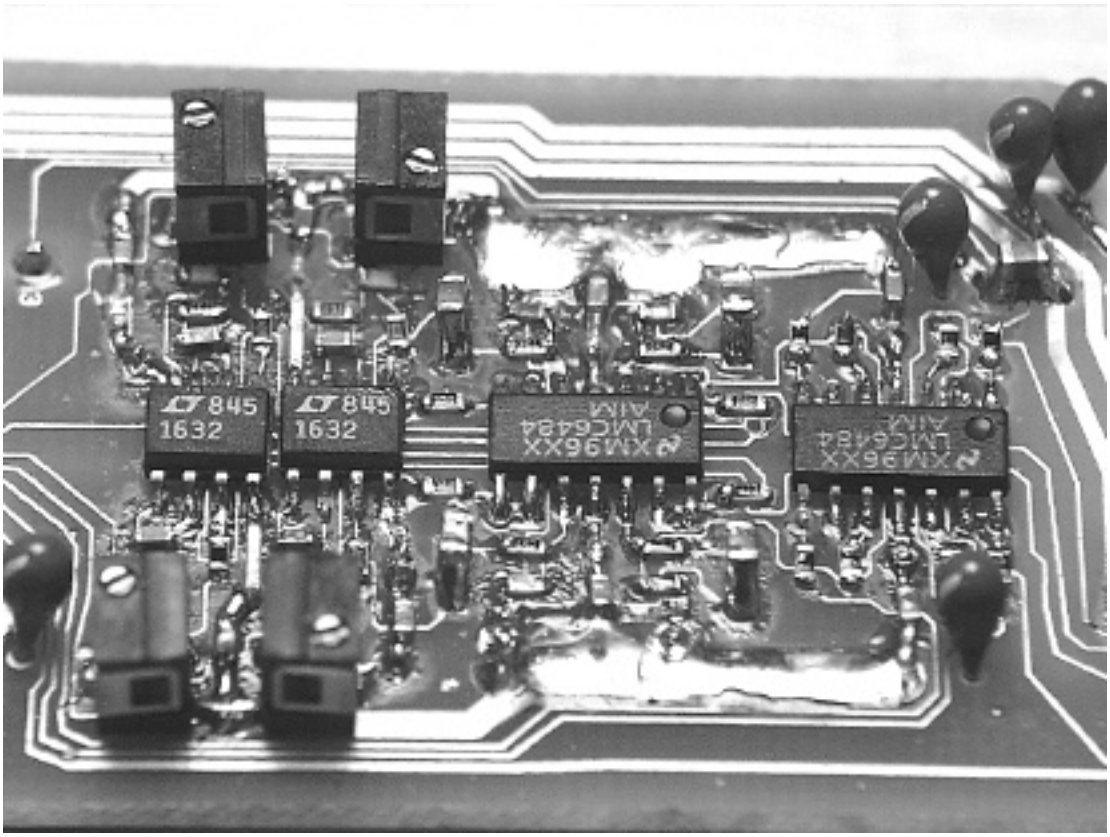

Fig. 21: A close-up of the current source components with their trimming potentiometers and feedback buffer IC in the middle. The recording output buffer IC is on the far right.

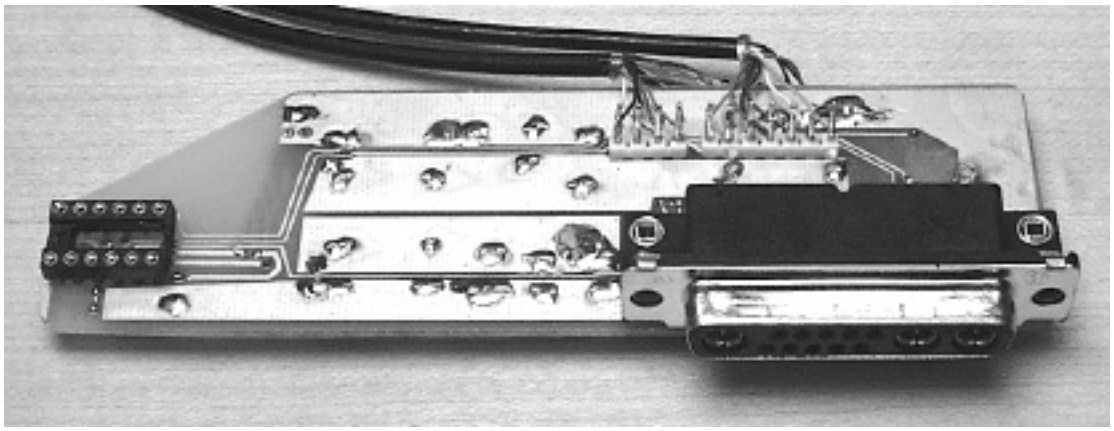

Fig. 22: The back side of the cable terminator/probe connector board shows the power supply buses and the various connectors and output pins.

3. Final Design of STIM-2

During the past quarter, we continued work to redesign STIM-2, our high-end 8-channel 64-site stimulating probe with on-chip current generation. The work has concentrated in the following areas:

1) On-chip DAC:

The digital-to-analog converter (DAC) is the most important circuit on the stimulating probe, STIM-2. Following previous work to optimize the DAC, a self-calibration technique has been explored as an alternative implementation. The basic principle is illustrated in Fig. 23. As S2 is closed and S1 is switched to I_{ref}, the transistor shown is connected as an MOS diode. The voltage V_{gs} on the intrinsic gate-source capacitance C_{gs} is determined by the transistor characteristics. When S2 is opened and S1 is switched to the output, the V_{gs} remains stored on the gate-to-source capacitance of the transistor; thus, the output current from the transistor will be equal to I_{ref}. Since any charge imbalance between the sourcing and sinking currents is a big concern in the DAC design, the separate current referencing in the original STIM-2 design can be avoided by using the sourcing current as the reference current for sinking current. Another advantage of this circuit is that only one transistor is needed for sinking a wide range of different current levels; thus, the charging of long gate rails of ratioed transistors can be eliminated.

The detailed DAC circuit is shown in Fig. 24. During the sourcing cycle, M7 is on while M6 and M8 are off. Here, the circuit works in the same way as that in the original STIM-2. Then, when M7 turns off and M6 turns on, the PMOS transistor rails M2-5 begin to charge the diode-connected M9, establishing a corresponding voltage on its large gate-to-source capacitance, C_{gs9}. After that, M6 is turned off and M8 is turned on, and the voltage across the gate and source of M9 will maintain the current flow and sink current from the site. Transmission gates M11-12 are added to cancel the charge

injection introduced by M10. M9 has a small transconductance to reduce the sensitivity of its current to small variations of its gate-to-source voltage. Due to the leakage currents at the drain-substrate junctions of M10-12, the charge stored on C_{gs9} decays with time, degrading the matching of the sinking current to the sourcing current. This is one limitation of this design; thus, the stimulation time can not be too long. The simulation results for this circuit are shown in Fig. 25. The sourcing and sinking currents are closely matched and the settling time during the sinking cycle is greatly improved.

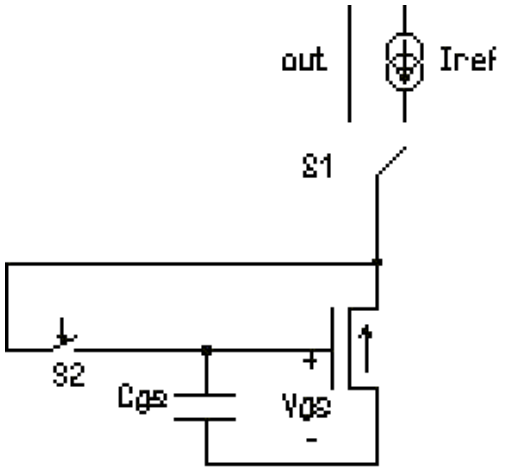

Fig. 23: Schematic of basic current calibration circuit.

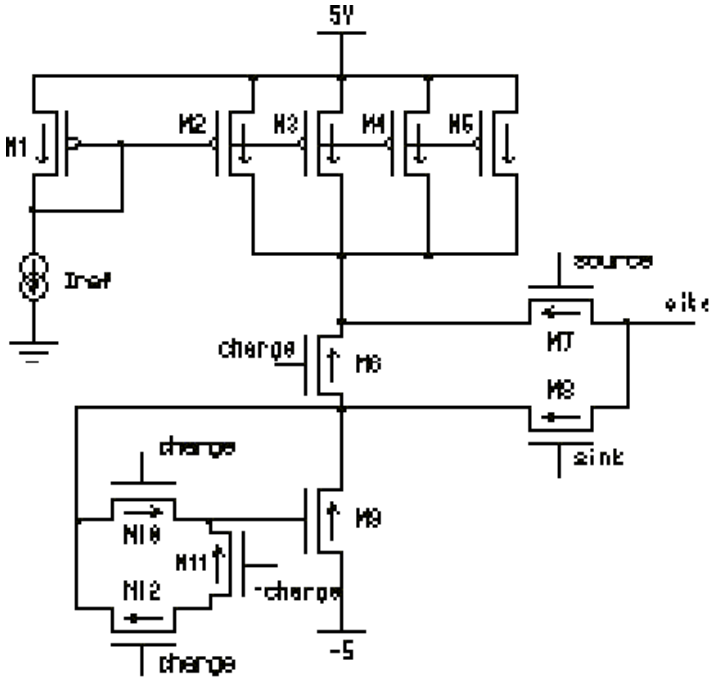

Fig. 24: Schematic of current cell with an output current 4X the I_{ref}

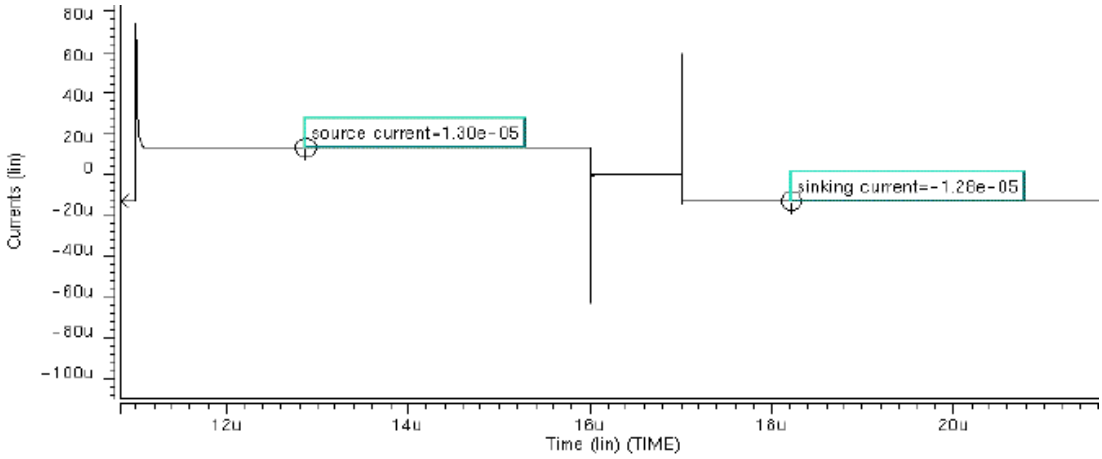

Fig. 25: Output sourcing and sinking currents 8X the I_{ref}

Although this design has a number of advantages over the previously used DAC, there are several concerns in implementing this design. First, as shown, the sourcing current is needed to charge the gate-to-source voltage to induce the sinking current; thus, strictly speaking, the charge delivery should be anodic-first instead of cathodic-first. A similar circuit, based on duality, could be used, however, to allow cathodic-first operation. Second, this design has the advantage of saving power consumption and layout area; however, it requires a somewhat different protocol than that used in the previous DAC design for STIM-2. Third, switching the selection transistors gives rise to disturbs, which cause changes in the gate voltage of M9 during switching. A current source having a value of about 90% of the source current could be added in parallel to M9 to decrease its current to about 10% and further reduce its transconductance. Finally, the voltage response of the stimulating site tends to rob the drive voltage of its ability to provide the desired current to a high-impedance load. Locally boosting the DAC drive voltage, e.g., with a charge pump, could be considered for high current delivery.

2) Addition of a Dedicated Data Path for Recording and Impedance Checking

Both the electrode impedance test mode and the recording mode require the resulting signal to be transmitted off-chip through the single data lead in STIM-2. Thus, these modes can not be performed during stimulation. For more general operation, an additional data path has been added and the control signal has been adjusted accordingly to allow the simultaneous monitoring of neural responses during stimulation.

3) A Multi-Level Anodic Bias

For higher charge delivery within the water window, anodic bias is desirable. STIM-2 has a mode which connects all unused sites to approximately 0.6V when specified by the user; however, a number of bias levels is preferred in the redesigned probe to allow for further research into electro-tissue coupling. A 4-bit DAC can be added to the probe to provide16 different voltage levels to the anodic bias setting with an

interval separation of 0.1V. Figure 26 illustrates a simple 2R-R resistive ladder D/A decoder. S1 is a sign switch to set the output reference voltage between - 0.8V(-Vref) and 0.8V (Vref) across the water window. S2-4 are bit switches to determine the specific output voltage across Rl. The main advantage of this type of decoder is that all the resistors are either R or 2R; thus, it is fairly easy to obtain resistors that are closely matched. A disadvantage is that the resistors take significant area.

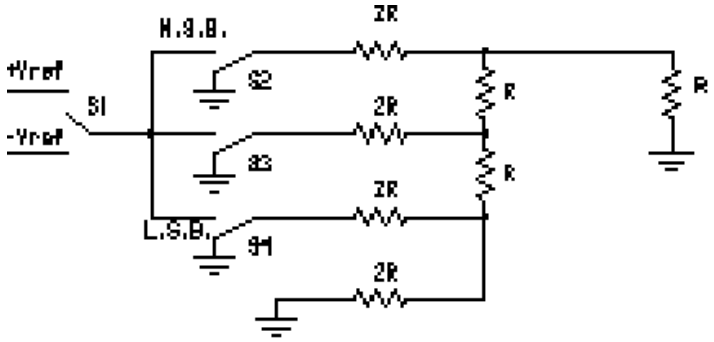

Fig. 26: Schematic of 2R-R ladder D/A decoder

We expect to complete the redesign of STIM-2 during the coming term. A 3D platform-based version of STIM-2 (STIM-3) will then be designed so that both probes can be fabricated during the remainder of the current year.

4. A Telemetry-Powered CNS Stimulating Microprobe

Present CNS stimulating probes (STIM-2, -2B/-3B) are not designed for use with telemetry but instead must be hardwired to the outside world through a percutaneous plug. We have started work to develop a platform-mounted probe interface to permit the percutaneous plug to be elimnated, providing rf power and input data to the implanted device and telemetering recorded signals to the outside world. In developing this interface, we are leveraging off of previous work done on wireless microstimulators for use in FNS. In these devices, we have used the fact that these stimulators are electrically isolated from the external world. Thus, bipolar stimulation can be used by applying the stimulus current differentially between two sites. The only difference between positive and negative stimulation is the direction of current flow between source and sink sites. This situation makes dual supplies unnecessary. Both positive and negative stimulating pulses can be applied by switching the current source and internal ground between different sites.

We are exploring the diffences between this configuration and the dual supply system used with present stimulating probes. Balanced dual supplies are, of course, simply a matter of where to set the internal tissue reference, and such a reference normally exists. In that sense, all stimulation is bipolar if the reference is included. We are comparing these two systems and are beginning to design various circuit blocks to implement the interface. We hope to have the first modules designed and ready for fabrication by the end of the coming term.

6. Conclusions

Recent activities in the development of active stimulating probes have focused on the external probe interface system and hardware. The graphical user interface (GUI) and probe drivers were updated to enable addressing of the 3D STIM-3B arrays in addition to the STIM-2B probes. The GUI prompts the user for the number of probes in the 3D array and configures the system accordingly. The input X- and Y-address data used to select the probe and the site on that probe are padded with extra bits to ensure they are of the same length and that the addresses will align properly in the input shift registers for reliable selection. Additional improvements are also being made to the software to make the system easier to use, in preparation for providing the system to outside users.

As part of the external probe stimulating system, a hardware interface has been built to facilitate current generation and recording on the headstage, avoiding the high distributed capacitance of the cables between the system and the preparation. The circuitry for a cable terminator/probe connector was designed and built on a printed circuit board (PCB). Current sources, a recording buffer, and a probe power supply current monitor were all included on the PCB for added flexibility and monitoring capability. The circuitry performs voltage-to-current conversion to generate the stimulus currents for STIM-2B/-3B, ensures charge-balancing, and provides a high drive impedance along with bias stabilization in recording mode. The output drive impedance (input recording impedance) as seen from the site is set by a fixed 100MΩ bias resistor. During the coming quarter, we expect to use the PCB to complete series of long term *in-vitro* pulse tests and to use it in *in-vivo* stimulation and recording experiments.

We are also continuing the final design optimization of STIM-2 and have explored a new self-balancing design for the digital-to-analog current sources needed for that probe. Dedicated data lines to permit recording during stimulation have been added along with a DAC to permit the use of up to 8 levels of anodic and cathodic bias on unused sites. The STIM-2 design should be completed during the coming term. STIM-3 will then be designed so that both probes can be fabricated before the end of the year. We are also beginning the design of a telemetry interface that will permit these probes to be operated over an rf power/data link, eliminating the need for a hardwired interface and percutaneous plug.